Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electrical and Electronics Engineering

BEE306Digital Electronics

Third Semester (Odd Semester)

Course (catalog) description

To develop a strong foundation in the field of Digital Electronics. The subject gives the students an in depth knowledge about Digital logic families, Combinational circuits and enable them to analyze and design any sequential circuits. Also this subject gives knowledge about various memory devices &VHDL

Compulsory/Elective course: Compulsory for EEE students

Credit hours& contact hours: 3 & 45 hours

Course Coordinator : Dr.V.Jayalakshmi

Instructors : Mr.K.Sakthivel

Name of the instructor	Class handling	Office location	Office phone	Email (domain:@ bharathuniv.ac.in	Consultation
Mr.K.Sakthivel	Second year EEE	KS 101	**04422290125**	Sakthivelk.eee@bharathuniv.ac.in	12.30-1.30 PM

Relationship to other courses:

Pre –requisites **:** BEE101 Basic Electrical & Electronics Engineering

Assumed knowledge : Basic knowledge in Logic gates, Boolean Techniques Digital circuits

Following courses : BEE403 Linear Integrated circuits

Syllabus Contents

UNIT I NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES 9

Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code-Digital Logic Families, comparison of RTL, DTL, TTL, ECL and MOS families -operation, characteristics of digital logic family.

UNIT II COMBINATIONAL CIRCUITS 9

Combinational logic - representation of logic functions-SOP and POS forms, K-map representation minimization using K maps - simplification and implementation of combinational logic – multiplexers and demultiplexers - code converters, adders, subtractors.

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS 9

Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters -asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits – Moore and Melay models- Counters, state diagram; state reduction; state assignment.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLELOGIC DEVICES 9

Asynchronous sequential logic circuits-Transition table, flow table-race conditions, hazards &errors in digital circuits; analysis of asynchronous sequential logic circuits-introduction to Programmable Logic Devices: PROM – PLA –PAL.

UNIT V VHDL 9

RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages –Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip flops, FSM, Multiplexers / Demultiplexers)

Text book(s) and/or required materials

T1. Raj Kamal, ' Digital systems-Principles and Design', Pearson Education 2nd edition, 2007.

T2. M. Morris Mano, 'Digital Design with an introduction to the VHDL', Pearson Education, 2013.

T3. Comer "Digital Logic & State Machine Design, Oxford, 2012.

Reference Books:

R1. Mandal "Digital Electronics Principles & Application, McGraw Hill,2nd edition,2013.

R2. Floyd and Jain, 'Digital Fundamentals', Pearson Education, 8th edition, 2003.

R3. Anand Kumar, "Fundamentals of Digital Circuits, PHI, 2nd edition ,2013.

R4. Charles H.Roth,Jr,LizyLizy Kurian John, 'Digital System Design using VHDL, Cengage, 2nd edition,2013.

R5. John M.Yarbrough, 'Digital Logic, Application & Design', Thomson, 3rd edition 2002.

R6. Gaganpreet Kaur, VHDL Basics to Programming, Pearson, 1 st edition2013.

1. **Computer usage:**http://nptel.ac.in/courses/117106086/1

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area :Circuit Theory | Electrical Machines| **Electronics** | Power System| Control &Instrumentation

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	August 1st week	Session 1 to 18	2 Periods
2	Cycle Test-2	September 2nd week	Session 19 to 36	2 Periods
3	Model Test	October 2nd week	Session 1 to 45	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

To develop a strong foundation in the field of Digital Electronics. The subject gives the students an in depth knowledge about Digital logic families, Combinational circuits and enable them to analyze and design any sequential circuits. Also this subject gives knowledge about various memory devices &VHDL	Correlates to program outcome		
	H	**M**	**L**
1. To study various number systems , simplify the logical expressions using Boolean functions	a,d,i	b,c,e,g,l	j,k
2. To study implementation of combinational circuits	a,d,e,I,l	b,c,g,l	j,k
3. To design various synchronous and asynchronous circuits	a,d,e,i	b,g,l	j,k
4. To introduce asynchronous sequential circuits and PLCs	a,d,e,i	b,g,l	j.k
5. To introduce digital simulation for development of application oriented logic circuits	a,d,e,	b,c,i,g,l	j,k

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture Schedule

S.NO	Topics	Problem solving (Yes/No)	Text / Chapter
UNIT I	**NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES**		
1.	Review of number systems	Yes	T1,T2
2.	binary codes	Yes	
3.	error detection and correction codes (Parity and Hamming code	No	
4.	error detection and correction codes (Parity and Hamming code	No	
5.	Digital Logic Families	Yes	
6.	Digital Logic Families	Yes	
7.	comparison of RTL, DTL, TTL, ECL and MOS families	No	
8.	comparison of RTL, DTL, TTL, ECL and MOS families	No	
9.	operation, characteristics of digital logic family.	No	
UNIT II	**COMBINATIONAL CIRCUITS**		
10.	Combinational logic	Yes	T1,T3,R2
11.	representation of logic functions-SOP and POS forms	Yes	
12.	K-map representation minimization using K maps	Yes	
13.	simplification and implementation of combinational logic	Yes	
14.	simplification and implementation of combinational logic	Yes	
15.	multiplexers and demultiplexers	Yes	
16.	multiplexers and demultiplexers	Yes	
17.	code converters, adders, subtractors.	Yes	
18.	code converters, adders, subtractors.	Yes	
UNIT III	**SYNCHRONOUS SEQUENTIAL CIRCUITS**		
19.	Sequential logic- SR, JK, Flip	Yes	T1,T2,R3
20.	flopsD and T flip flops -.	Yes	
21.	level triggering and edge triggering	Yes	
22.	counters -asynchronous and synchronous type	Yes	
23.	Modulo counters	Yes	
24.	Shift registers	Yes	
25.	design of synchronous sequential circuits	Yes	
26.	Moore and Melay models	No	
27.	Counters, state diagram; state reduction; state assignment	Yes	
UNIT IV	**ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLELOGIC DEVICES**		
28.	Asynchronous sequential logic circuits	Yes	
29.	Transition table,	No	

30.	flow table-race conditions,	Yes	
31.	hazards &errors in digital circuits;	Yes	
32.	analysis of asynchronous sequential logic circuits	Yes	
33.	analysis of asynchronous sequential logic circuits	No	
34.	introduction to Programmable Logic Devices: PROM	No	T3,R2
35.	introduction to Programmable Logic Devices: PLA	Yes	
36.	introduction to Programmable Logic Devices:–PAL	No	
UNIT V VHDL			
37.	RTL Design	No	
38.	RTL Design	No	
39.	combinational logic	Yes	
40.	Sequential circuit	Yes	
41.	Operators	No	
42.	Introduction to Packages	Yes	T1,T2
43.	Subprograms	No	
44.	Test bench. (Simulation /Tutorial Examples: adders	Yes	
45.	Test bench. (Simulation /Tutorial Examples: adders	Yes	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures
- Tutorials, which allow for exercises in problem solving and allow time for students to resolve problems in understanding of lecture material.
- Laboratory sessions, which support the formal lecture material and also provide the student with practical construction, measurement and debugging skills.
- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	05%
Cycle Test – II	-	05%
Model Test	-	10%
Attendance	-	05%
SEMINAR&ASSIGNMENT		05%
Final exam	-	70%

Prepared by: K.Sakthivel Associate Professor, Department of EEE **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / EEE / program by the time that they graduate:

a) An ability to apply knowledge of mathematics, science, and engineering fundamentals.

b) An ability to identify, formulate, and solve engineering problems.

c) An ability to design a system, component, or process to meet the desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.

d) An ability to design and conduct experiments, as well as to analyze and interpret data.

e) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

f) An ability to apply reasoning informed by the knowledge of contemporary issues.

g) An ability to broaden the education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.

h) An ability to understand professional and ethical responsibility and apply them in engineering practices.

i) An ability to function on multidisciplinary teams.

j) An ability to communicate effectively with the engineering community and with society at large.

k) An ability in understanding of the engineering and management principles and apply them in project and finance management as a leader and a member in a team.

l) An ability to recognize the need for, and an ability to engage in life-long learning.

Program Educational Objectives

PEO1: PREPARATION
Electrical Engineering Graduates are in position with the knowledge of Basic Sciences in general and Electrical Engineering in particular so as to impart the necessary skill to analyze and synthesize electrical circuits, algorithms and complex apparatus.

PEO2: CORE COMPETENCE
Electrical Engineering Graduates have competence to provide technical knowledge, skill and also to identify, comprehend and solve problems in industry, research and academics related to power, information and electronics hardware.

PEO3: PROFESSIONALISM
Electrical Engineering Graduates are successfully work in various Industrial and Government organizations, both at the National and International level, with professional competence and ethical administrative acumen so as to be able to handle critical situations and meet deadlines.

PEO4: SKILL
Electrical Engineering Graduates have better opportunity to become a future researchers/ scientists with good communication skills so that they may be both good team-members and leaders with innovative ideas for a sustainable development.

PEO5: ETHICS
Electrical Engineering Graduates are framed to improve their technical and intellectual capabilities through life-long learning process with ethical feeling so as to become good teachers, either in a class or to juniors in industry.

Course Teacher	Signature
K.Sakthivel	

Course Coordinator **HOD/EEE**

(K.Sakthivel)